ECE 424

Lab 6

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I. Introduction

In Lab 6, we were introduced to VHSIC Hardware Description Language. After learning the basic syntax and rules of the language, we reconstructed the ALU from a previous lab, using our newfound knowledge. The learning curve for VHDL was initially steep, but after diving into the provided documents, the curve became more manageable. Overall, the lab was difficult due to the plethora of new information.

II. Procedure

Most of the time on Lab 6 was spent scanning the provided VHDL Primer document. After reading the lab documentation, I realized that the instructions were extremely similar to a previous lab. I consulted the .bdf file for lab 4 in order to get a better understanding of the specifications of the ALU. After I had a general understanding of the input, circuit logic, and outputs of the proposed ALU, I consulted the VHDL Primer document.

Although the reading was dry, the document was extremely helpful in completing the lab. I read the document in its entirety one time, and then created a VHDL file on quartus. I was not exactly sure where to start. After several attempts and failed compilations, I read the document in its entirety again. I then began developing a 4 to 1 multiplexer with two select inputs. Initially, the logic for the multiplexer was written inside a process, but during a recent class period, Dr. Choi mentioned that we should avoid using processes at all costs. Instead, I opted to created some internal variables and use “when else” statements after assigning the required logic to the created variables. After writing my VHDL code (Figure 1), I complied and ran a functional simulation (Figure 2).

After the code was successful, I created a symbol and then created a .bdf file in order to implement the seven segment decoder. Using previous knowledge the block diagram was created, compiled, and programmed relatively quickly.

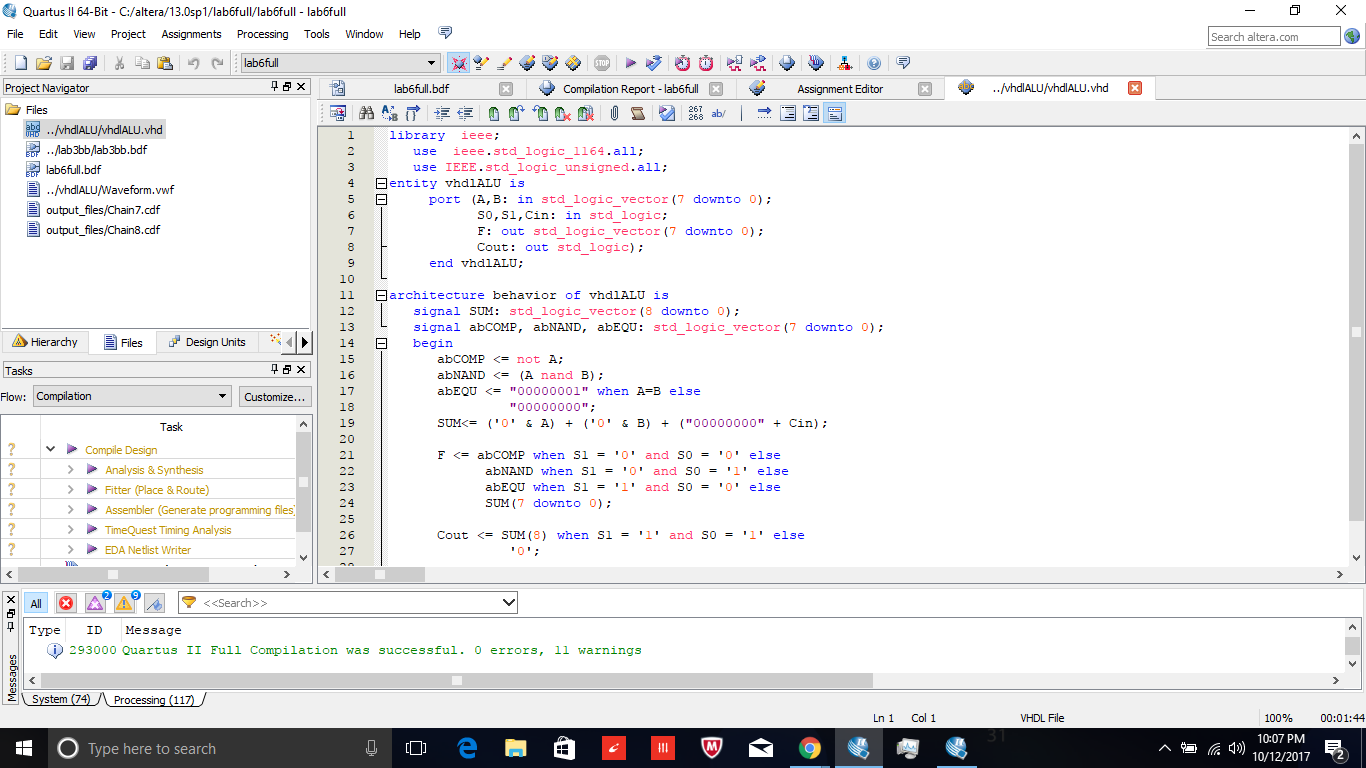


Figure 1: VHDL File

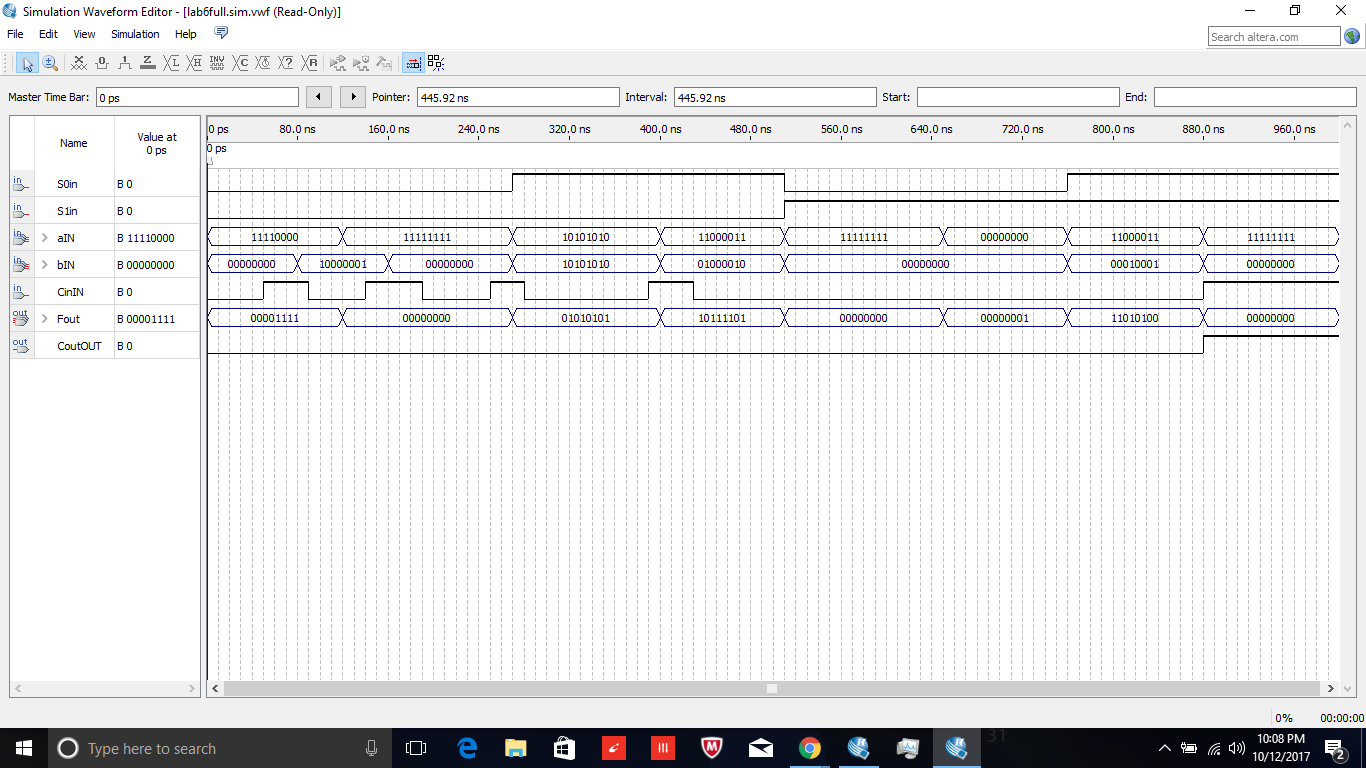


Figure 2: Functional Simulation

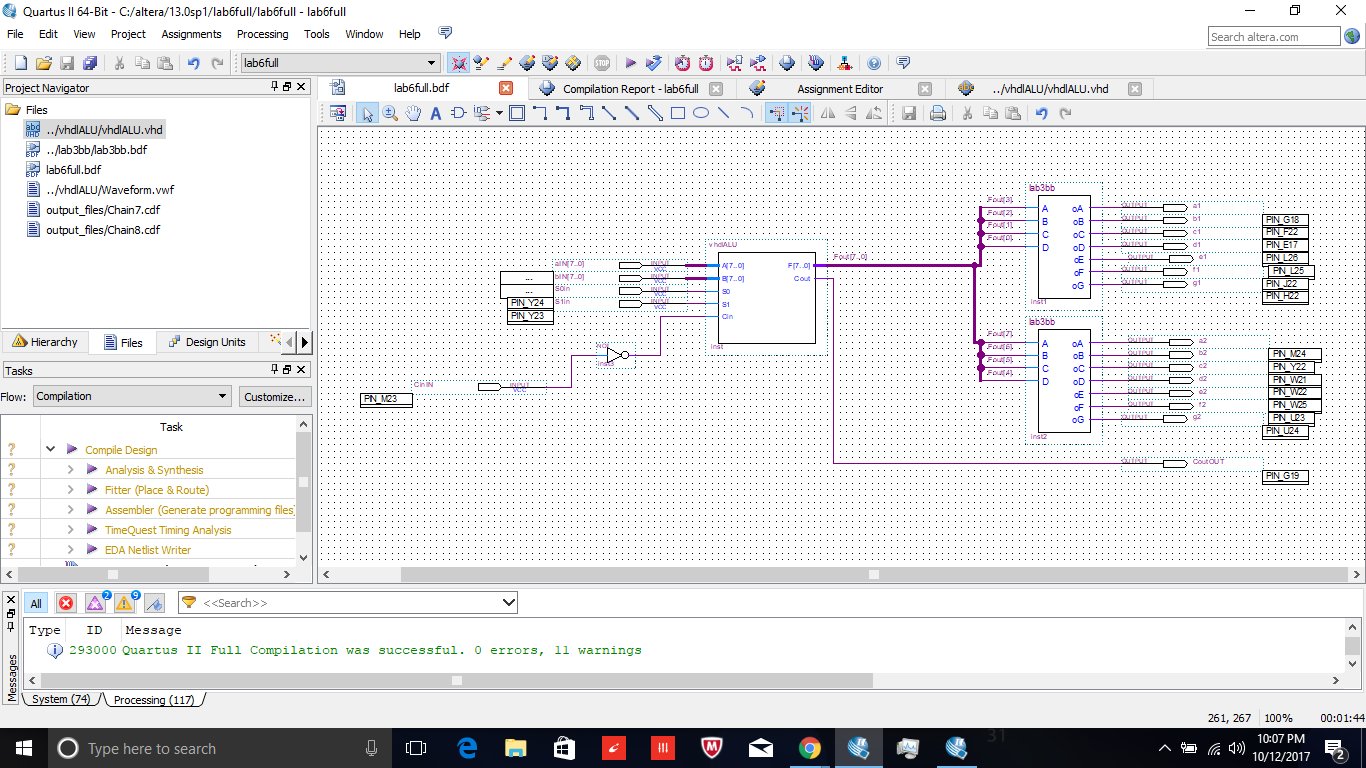


Figure 3: ALU Block Diagram

III. Conclusion

Overall, the lab was difficult due to the amount of learning involved. There was quite a bit of new information presented in this lab. It took me a little while to grasp the basic concepts of VHDL. Some of the code was similar to C, but the structure is very different from most of the programming that I have done in the past. I am looking forward to expanding my knowledge of VHDL in future, more complex labs.